# Control Loop in TOSCA PoC

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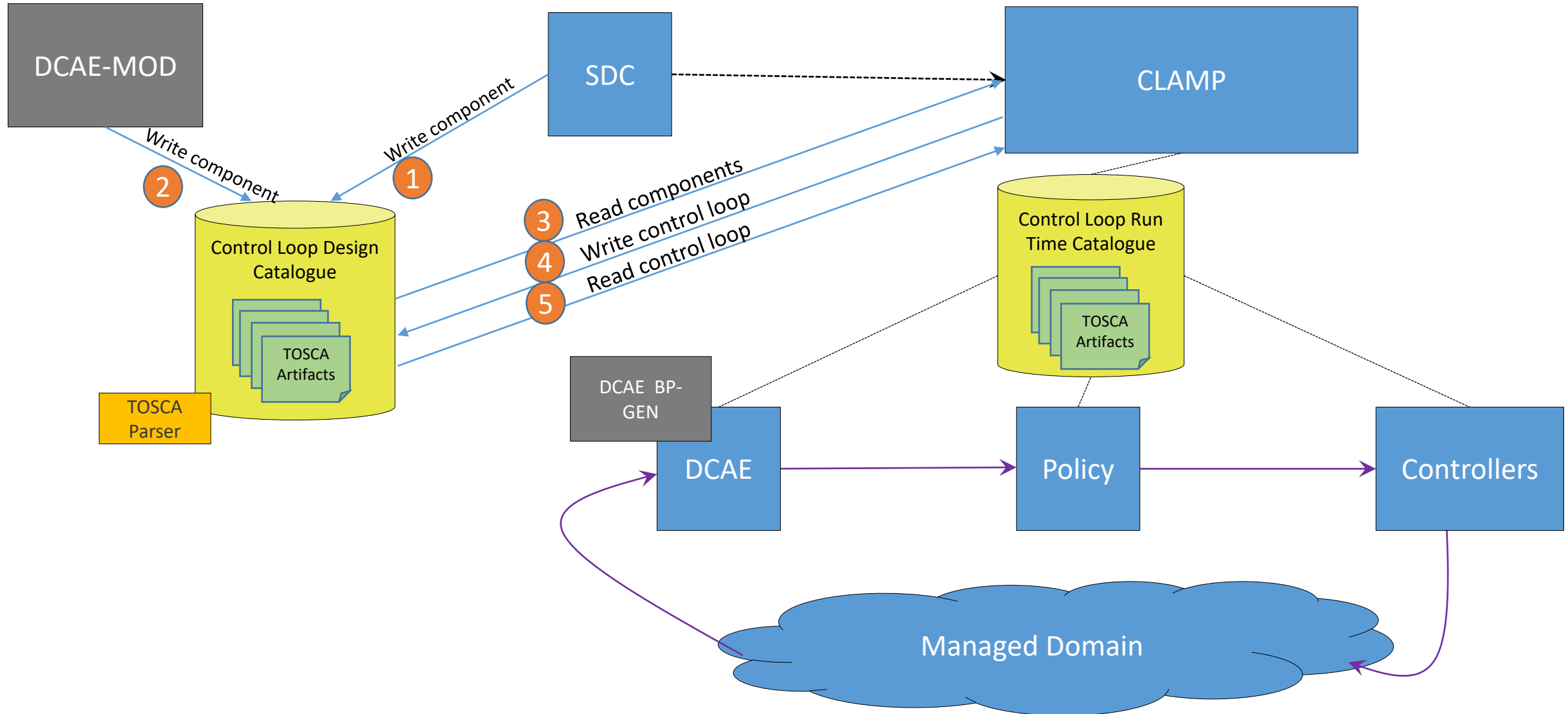Pamela Dragosh, Vijay V Kumar, Scott Blandford – AT&T

# Control Loop in TOSCA PoC - Background

- A first Control Loop in TOSCA proposal shared in Jan 2020, ONAP Prague Event

- Control Loop in Tosca (BGP in Tosca) is a ONAP Rel G requirement from Control Loop Subcommittee.

- Topic under discussion in ONAP Control Loop Subcommittee for more than 1 month involving CLAMP, Policy and DCAE experts

- A PoC to start to experiment the use of TOSCA artifacts describing Control Loop and Controlo Loop components: REQ-402
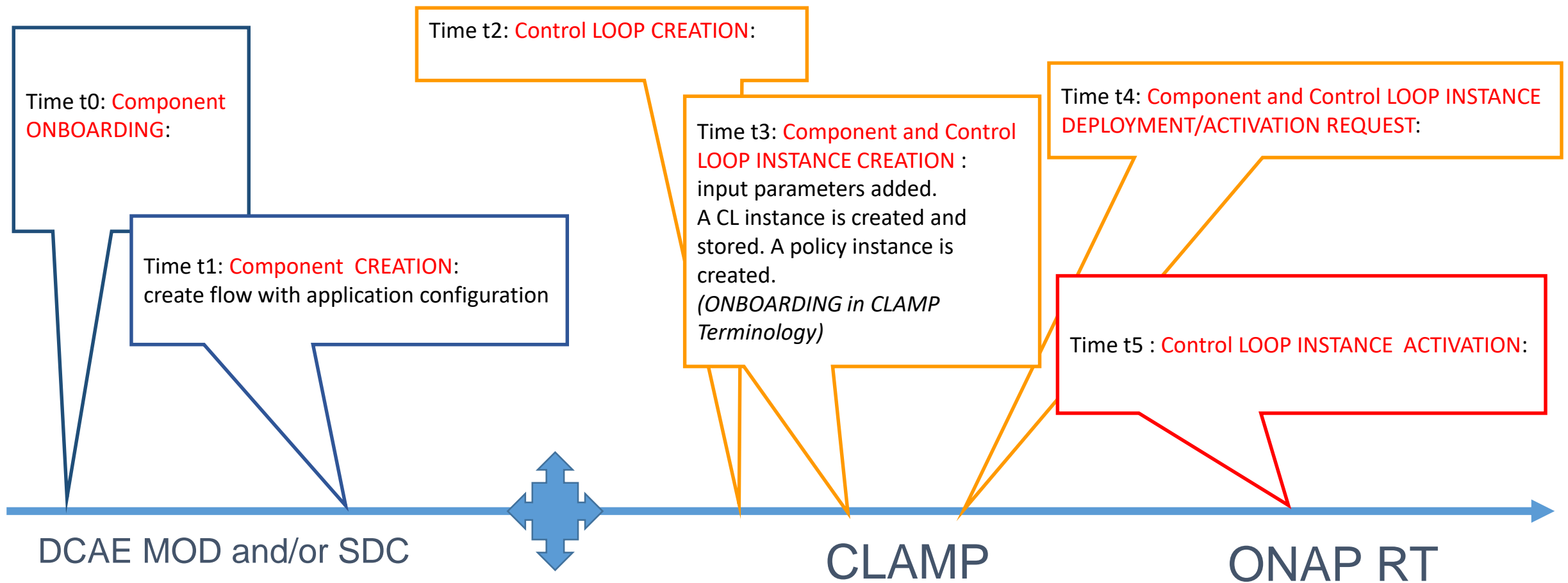
# Guilin: TOSCA Defined Control Loop – Overall Goals

- Demonstrate Control loops defined and deployed using TOSCA

- Use a design time catalogue for Control Loops for a complete storage of all the artifacts from different DT systems

- Show design time systems can populate the Design Time control loop catalogue
  - DCAE-MOD interacting with the design time catalogue
  - SDC interacting with the design time catalogue

- Show TOSCA defined control loops being onboarded and deployed

# Control Loop Artifacts in TOSCA and Design Catalogue Iterations

# Control Loop Timeline

Time t0: Component ONBOARDING:

Time t1: Component CREATION:
create flow with application configuration

Time t2: Control LOOP CREATION:

Time t3: Component and Control LOOP INSTANCE CREATION :
input parameters added.
A CL instance is created and stored. A policy instance is created.
(ONBOARDING in CLAMP Terminology)

Time t4: Component and Control LOOP INSTANCE DEPLOYMENT/ACTIVATION REQUEST:

Time t5 : Control LOOP INSTANCE  ACTIVATION:

DCAE MOD and/or SDC

CLAMP

ONAP RT

# Guilin: TOSCA Defined Control Loop - Stories

1. Create a TOSCA definition for a Control Loop (and its components)

2. Create Design Time Catalogue for control loops

3. Create REST interface towards Design Time Catalogue

4. Build interaction between SDC and Design Time Catalogue

5. Build interaction between DCAE-MOD and Design Time Catalogue

6. Build interaction between Design Time Catalogue and Run Time CLAMP