Supported HPA Capability Requirements(DRAFT)

⚠ The plan is to move this content over to ETSI for standardization as a ETSI SOL NFV Registry

VDU CPU Requirements

Property in tosca.datatypes.nfv.VirtualCpu contained in tosca.capabilities.nfv.VirtualCompute

Capability Name	Capability Value	Generic Capability	Description
cpuModelSpecificationBinding	strictBinding equalOrBetterBinding	✅	VDUs may be developed, compiled, optimized or validated on particular CPU models. Some deployments may wish to permit the VDU to be deployed on a platform with the specified CPU only, or with an alternative CPU with the same architecture, instruction set, and if specified, instruction set extensions, or with a CPU of equivalent or greater capability.
instructionSetRequirements	aes, sse, avx, cat, cmt, mbm, ddio, smt, rdrand, etc etc	✅	Long list of instruction set extensions.
simultaneousMultiThreading	Enabled disabled	✅	The use of Simultaneous Multi-Threading HW is an efficient way to increase the compute capacity of a platform. SMT HW threads share some CPU core resources. In some VDU implementations, it may be necessary to very explicitly control the HW thread allocation on a platform. This could be to help ensure locality in data caches or as a mechanism to enhance determinism
hypervisorConfiguration	HPET memoryCompaction kernelSamepageMerging	✅	Long list: High Precision Event Timer configuration, memory compaction, kernel samepage merging, etc.
computeRas	pciDetectedAndCorrectedErrors pciDetectedAndUncorrectedErrors	✅	Reliability, Availability, Serviceability (RAS) Long list of values: pciDetectedAndCorrectedErrors, pciDetectedAndUncorrectedErrors
cpuModel	List of model identifiers		The CPU model for which the VDU has been developed, compiled for, optimized on, validated on or preferred for some reason.
directIoAccessToCache	Values – TBD		Descriptions related to cache functions – TBD
accelerator	Values – TBD		Descriptions related to accelerator functions – TBD
measuredLaunchEnvironment	Values – TBD		Descriptions related to boot environment functions – TBD
secureEnclave	Values – TBD		Descriptions related to secure region functions – TBD
numVirtualCpu	1-N		Number of virtual CPUs
virtualCpuClock	0-N		Minimum virtual CPU clock rate (e.g. in MHz). The cardinality can be 0 during the allocation request, if no particular value is requested.
logicalCpuPinningPolicy	dedicated shared		Determines if CPUs from the host platform should be committed to the VDU or shared between VDUs.
logicalCpuThreadPinningPolicy	require isolate prefer		Determines the manner in which CPU (HW) threads are allocated to VDUs. Require means CPU (HW) thread siblings should be allocated Isolate means allocate CPU (HW) threads from different execution units. Prefer means ideally allocate CPU HW threads from the same physical execution units but if not available, continue with allocation.

VDU Memory Requirements

Property in tosca.datatypes.nfv.VirtualMemory contained in tosca.capabilities.nfv.VirtualCompute

Capability Name	Capability Value	Description
memoryPageSize	ANY, 4KB, 2MB, 1GB	Memory page size
numberOfPages	0..N	Number of pages of this specific page size. Note, The size of memory requested in all instances of the vduMemRequirements must be less than or equal to the virtualMemSize attribute of the virtualMemoryData information element.
memoryAllocationPolicy	strictLocalAffinity preferredLocalAffinity	Strict Local (to node) Affinity or Preferred local (to node) affinity
memoryType		Type of memory
memorySpeed		Agreed unit of memory speed
memoryRas	ECC, SDDC, thermalThrottling, demandAndPatrolScrubbing	Long list of memory technologies
memoryBandwidth	0..N	Agreed unit of memory bandwidth where 0 is unspecified.
processorCacheAllocationType	Values – TBD	Agreed type of processor cache allocation
processorCacheAllocationSize	0..N	Agreed unit of processor cach

VDU Storage Requirements

Property in tosca.nodes.nfv.Vdu.VirtualStorage

Capability Name	Capability Value	Description
storageIops	0..N	Required storage characteristics (e.g. speed), including Key Quality Indicators (KQIs) for performance and reliability/availability
storageResilencyMechanism	Erasure tripleReplication	Erasure code based back-end, triple replication based back-end for ensuring data resiliency.

Logical Node Compute Requirements

Property Logical Node Requirements in tosca.datatypes.nfv.LogicalNodeData contained in tosca.capabilities.nfv.VirtualCompute

Capability Name	Capability Value	Description
numberCpu	0..N	Number of CPU cores for this logical node. The cumulative number of CPU requests per node must equal the VDU level numVirtualCpu requirement.

Logical Node Memory Requirements

Property Logical Node Requirements in tosca.datatypes.nfv.LogicalNodeData contained in tosca.capabilities.nfv.VirtualCompute

Capability Name	Capability Value	Description
localNumaMemorySize	0..N	The amount of memory that needs to be collocated with this specific logical (NUMA) node.

Logical Node i/O Requirements

Property Logical Node Requirements in tosca.datatypes.nfv.LogicalNodeData contained in tosca.capabilities.nfv.VirtualCompute

Capability Name	Capability Value	Description
pciVendorId		PCI-SIG vendor ID for the device
pciDeviceId		PCI-SIG device ID for the device
pciNumDevices		Number of PCI devices required.
pciAddress		Geographic location of the PCI device via the standard PCI-SIG addressing model of Domain:Bus: device:function
pciDeviceLocalToNumaNode	required notRequired	Determines if I/O device affinity is required.

Network Interface Requirements

Property in tosca.datatypes.nfv.VirtualNetworkInterfaceRequirements contained in tosca.nodes.nfv.VduCp

Capability Name	Capability Value	Description
nicFeature	LSO, LRO, RSS, RDMA	Long list of NIC related items such as LSO, LRO, RSS, RDMA, etc.
dataProcessingAccelerationLibrary	Dpdk	Name of the data processing acceleration library required. Orchestration can match any NIC that is known to be compatible with the specified library.
dataProcessingAccelerationLibraryVersion	Version	Version of the data processing acceleration library required. Orchestration can match any NIC that is known to be compatible with the specified library.
interfaceType	Virtio, PCI-Passthrough, SR-IOV, E1000, RTL8139, PCNET	Network interface type
vendorSpecificNicFeature	TBA	List of vendor specific NIC related items.